

## SP-ETHERNET Datasheet v1.0



## **Features:**

- Connect to the board through the SP-MOD SPI interface
- Master chip: The W5500 chip is a Hardwired TCP/IP embedded Ethernet controller
- The theoretical SPI design speed is 80MHz
- 10BaseT/100BaseTX Ethernet PHY embedded, Supports Auto Negotiation (Full and half duplex, 10 and 100-based ) Size :35\*20mm
- Connection method: SP-MOD (2\*4P 2.54mm pin header)

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UPDATE	
V1.0	2019/4/22; Published original document

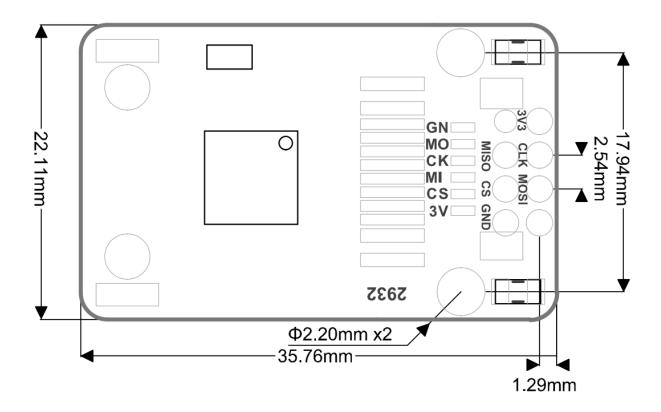
	INTRODUCTION
	Supply voltage of external power supply : 2.97V~3.63V
	Supply current of external power supply: <132mA
	Sleep Status of Current: <15mA
	TCP/IP protocol, Support
	TCP,UDP,ICMP,IPv4,ARP,IGMP,PPPoE protocols
	The theoretical SPI design speed is 80MHz
Chip: W5500	Supports 8 independent sockets simultaneously
	Internal 32Kbytes Memory for TX/RX Buffers
	Supports Wake on LAN over UDP
	10BaseT/100BaseTX Ethernet PHY embedded
	Support Auto Negotiation (Full and half duplex, 10 and 100-
	based )
	Not support auto-MDIX feature

HARDWARE FEATURES			
Supply voltage of external power supply	2.6V~3.6V		
Supply current of external power supply	<132mA		
Temperature rise	<30K		
Range of working temperature	-40°C ~ 85°C		

SIZE		
Length	35.76mm	
Width	19.74mm	
Height	15.56 mm (Excluding the height of pin header: 8.7mm)	

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PIN DESCRIPTION		
1	GND	Ground
2	cs	Chip Select input pin
3	SO	Master In Slave Out
4		Not connected
5	3V3	Power supply(3.3V)
6	SCK	SPI clock pin
7	SI	Master Out Slave In
8		Not connected

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RESOURCES		
Official Website	www.sipeed.com	
Github	https://github.com/sipeed	
BBS	http://bbs.sipeed.com	
Wiki	maixpy.sipeed.com	
Sipeed Model Store	https://maixhub.com/	
SDK Reference	dl.sipeed.com/MAIX/SDK	
HDK Reference	dl.sipeed.com/MAIX/HDK	
E-mail(Technical Support)	support@sipeed.com	
Telgram Link	https://t.me/sipeed	
QQ Group	878189804	



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